CLAIMS:

1. Method of manufacturing a semiconductor device (10) comprising a field effect transistor, in which method a semiconductor body (1) of silicon is provided at a surface thereof with a source region (2) and a drain region (3) of a first conductivity type, which regions are both provided with extensions (2A,3A), and with a channel region (4) of a second conductivity type, opposite to the first conductivity type, between the source region (2) and the drain region (3), and with a gate region (5) separated from the surface of the semiconductor body (1) by a gate dielectric (6) and situated above the channel region (4), and wherein a pn-junction between the extensions (2A,3A) and a neighboring part (4A) of the channel region (4) is formed by two implantations (I_1, I_2) of dopants of opposite conductivity type, and wherein before both of said two implantations (I_1, I_2) of dopants of opposite conductivity type are performed an amorphizing implantation (I_0) is performed where the pn-junction is to be formed, characterized in that the amorphizing implantation (I_0) and said two implantations (I_1, I_2) of dopants of opposite conductivity type are performed before the gate region (5) is formed and at an angle with the surface of the semiconductor body (1) which is substantially equal to 90 degrees.

2. Method according to claim 1, characterized in that a first implantation (I_1) of said two opposite conductivity type implantations (I_1, I_2) is carried out using a first mask (M1) covering a first region of the semiconductor body (1) and the second implantation (I_2) is carried out after removal of the first mask (M1), using a second mask (M2) of which the edge coincides with the edge of the first mask (M1).

3. Method according to claim 2, characterized in that the first mask (M1) and the second mask (M2) are formed in a self-aligned manner.

4. Method according to claim 2 or 3, characterized in that the first mask (M1) is formed by a dummy gate region (5A) of a first dielectric material, and the first implantation (I_1) is used to form the extensions (2A,3A) of the source and drain regions (2,3).

5. Method according to claim 4, characterized in that after the first implantation (I_1) a uniform masking layer (40) of a second dielectric material different from the first dielectric material is deposited on the semiconductor body (1) and is subsequently removed by chemical mechanical polishing from the top of the dummy gate region (5A) which is then removed by selective etching, the remainder of the masking layer (40) forming the second mask (M2) for the second implantation (I_2) which is used to dope the neighboring part (4A) of the channel region (4).

6. Method according to claim 5, characterized in that, after the second implantation (I_2), a uniform gate region layer (50) is formed on top of the semiconductor body (1) and is subsequently removed by chemical mechanical polishing from the top of the second mask (M2) which is then removed by selective etching.

7. Method as claimed in any one of the preceding claims, characterized in that the first and second implantations (I_1 , I_2) are annealed at a temperature between 500 en 700 degrees Celsius

8. Method as claimed in any one of the preceding claims, characterized in that the source- and drain regions (2,3) are formed before the source- and drain extensions (2A,3A).

9. Method as claimed in any one of the preceding claims, characterized in that for the amorphizing implantation (I_0) ions are chosen from a group comprising Ge, Si, Ar or Xe.

10. Method as claimed in any one of the preceding claims, characterized in that a part of the function of the amorphizing implantation (I_0) is provided by one of the two opposite conductivity type implantations (I_1 , I_2).

11. A semiconductor device (10) comprising a field effect transistor obtained with a method as claimed in any one of the preceding claims.